first semiconductor die being attached to each of the leads;

a second semiconductor die including a plurality of bond pads disposed thereon, the second semiconductor die being attached to the first semiconductor die;

means for electrically connecting the bond pads of the first and second semiconductor dies to respective ones of the leads; and

an encapsulating portion applied to and at least partially encapsulating the leads, the first and second semiconductor dies, and the electrical connection means.

20. (New) The semiconductor package of Claim 19 wherein the electrical connection means comprises conductive wires.

21. (New) The semiconductor package of Claim 20 wherein:

each of the leads defines opposed first and second surfaces and a third surface which is opposed to the second surface and oriented between the second and third surfaces;

the bond pads of the first semiconductor die are electrically connected to respective ones of the first surfaces of the leads by respective ones of first conductive wires; and

the bond pads of the second semiconductor die are electrically connected to respective ones of the second surfaces of the leads by respective ones of second conductive wires.

22. (New) The semiconductor package of Claim 21 wherein the encapsulating portion is applied to the leads such that the third surface of each of the leads is exposed within the encapsulating portion.

23. (New) The semiconductor package of Claim 19 further comprising:

a die paddle, the leads being disposed about the die paddle;

the first semiconductor die being attached to the die paddle.

24. (New) The semiconductor package of Claim 23 wherein:

the die paddle defines opposed top and bottom surfaces, with the first semiconductor die being attached to the top surface of the die paddle; and

the encapsulating portion is applied to the die paddle such that the bottom surface of the die paddle is exposed within the encapsulating portion.

25. (New) The semiconductor package of Claim 19 wherein the first semiconductor die and the leads are oriented relative to each other such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact any one of the leads.